PTOCLM

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AS

CLAIMS 1-10(CANCELLED)

Claim 11 (currently amended). A control loop, comprising:

a phase shifter for producing an output with a first clock phase;

a phase detector for detecting a phase difference between a second clock phase of a data signal and the first clock phase,

said phase detector producing an output signal based on the detected phase difference;

a charge pump for integrating the output signal of said phase detector, said charge pump producing a ~~regulation signal~~ control voltage for said phase shifter; and

said phase shifter changing over a phase regulation direction ~~at predetermined switching points based on said regulation signal~~ when the control voltage reaches an upper or a lower range limit thereof;

said changing over of said phase regulation direction being performed with a hysteresis behavior.

Claim 12 (previously presented). The control loop according to claim 11, in combination with a delay locked loop circuit, said delay locked loop circuit having a delay locked loop control loop including said phase shifter, said phase detector, and said charge pump.

Claim 13 (currently amended). A method for producing a clock signal, which comprises:

detecting a phase difference between a clock phase of a first input signal and a clock phase of a first output signal of ~~the~~ a phase shifter;

producing a second output signal based on the detected phase difference;

producing a ~~second input signal~~ control voltage for the phase shifter by integrating the second output signal; and

changing a phase regulation direction of the phase shifter ~~at predetermined switching points based on the second input signal~~ when the control voltage reaches an upper or a lower range limit thereof, the changing over of the phase regulation direction being performed with a hysteresis behavior.

Claim 14 (currently amended). A phase shifter for producing an output signal, which comprises:

a circuit for receiving an input signal having a phase and for receiving a control voltage within a voltage range;

said circuit ~~also~~ being configured for producing an output signal having a phase , the phase of the output signal being controlled by the control voltage;

said circuit ~~designed~~ being configured for changing a phase regulation direction of the phase shifter when the control voltage reaches an upper or a lower range limit thereof;

~~at predetermined switching points based on an input signal,~~ ~~the~~ wherein the changing over of the phase regulation direction ~~being~~ is performed with a hysteresis behavior.

Claims 15-17 (canceled).